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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, April 2015
(2013 Scheme)
13.304 : ANALOG ELECTRONICS (E)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **2** marks.

1. Draw the circuit for a collector feedback bias for CE configuration.
2. Explain the need for bias stabilization.
3. In a transistor circuit, load resistance is 6 KΩ and quiescent current is 1.5 mA. Determine the operating point, when the battery voltage V_{cc} = 12V. What is the change in Q point when the load resistance is changed from 5 KΩ to 7.5 KΩ ?
4. Explain the parameters of JFET.
5. What are the advantages of CMOS devices ?
6. Give one application for
   i) Transformer coupled amplifier
   ii) Direct coupled amplifier.
7. Explain the difference between a voltage amplifier and a power amplifier.
8. What is meant by cross over distortion in amplifiers ?
9. Explain drift compensation in 741C op-amp.
10. Explain the following terms with respect to op-amp
    i) CMRR
    ii) Input bias current.

(10×2=20 Marks)

P.T.O.

PART – B

Answer **one full** question from **each** Module. **Each** question carries **20** marks.

Module – I

11. a) Design a voltage divider bias circuit for an NPN transistor having $h_{fe} = 120$ and $V_{BE} = 0.7$ V. The desired Q point is $V_{CE} = 5$ V and $I_c = 1$mA and stability factor should be less than or equal to 7. $V_{cc} = 10$ V and $R_E = 1\ K\Omega$. **12**

    b) Explain diode compensation for V_{BE} in a transistor circuit. **8**

12. a) Draw the h parameter equivalent circuit of a loaded amplifier in CE configuration and derive the expressions for current gain, voltage gain, input impedance, overall voltage gain and current gain. **15**

    b) Explain the significance of using h parameters. Also state the limitations of it. **5**

Module – II

13. a) Obtain the expressions for voltage gain, input impedance and output impedance of common drain JFET amplifier using small signal model. **15**

    b) The transconductance of an FET used as a voltage amplifier circuit (common source amplifier) is 2500 μ s and the load resistance is 12 $K\Omega$. Determine the voltage gain of the amplifier circuit. Take rd and $R_D >> R_L$. **5**

14. a) Explain in detail, the difference in construction and characteristics of depletion and enhancement type MOSFET. **10**

    b) Draw the circuit and explain the working of a transformer coupled transistor amplifier. **10**

Module – III

15. a) Show that the maximum efficiency of a transformer coupled class A power amplifier is 50%. 12

    b) A transformer coupled class A power amplifier draws a current of 150 mA from a collector supply of 10 V, when no signal is applied to it. Determine

    i) Maximum output power

    ii) Maximum collector efficiency and

    iii) Power rating of the transistor. 8

16. a) Explain the working of an RC phase shift oscillator, with a neat circuit diagram. Also derive the expression for frequency of oscillation. 15

    b) To an amplifier of 60dB gain, a negative feedback of $\beta = 0.006$ is applied. What would be the change in the overall gain of the feedback amplifier if the gain of the amplifier decreases by 15% ? 5

Module – IV

17. a) Draw the block diagram of an op-amp and explain the operation of each block. 5

    b) i) Explain the differences between IC op-amps 741 and 301. 5

    ii) Design and implement the following circuit with two operational amplifiers $V_o = -5V_1 + 2V_2 - 10V_3$. Use minimum value of resistance as 10 KΩ. 10

18. a) i) Explain the working of an op-amp integrator with neat diagram. 5

    ii) A 12 mV, 2 kHz sinusoidal signal is applied to the inverting input terminal of an op-amp integrator for which R = 50 KΩ and C = 2μf. Determine the output voltage. 5

    b) With neat diagram and relevant waveforms, explain the working of a voltage level detector. 10